HM514256API/AJPI/AZPI-6/7/8/10/12 — Preliminary
(Extended Temperature Range Version)

262,144-Word × 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514256A is a CMOS dynamic RAM organized 262,144-word × 4-bit. HM514256A has realized higher density, higher performance and various functions by employing 1.3μm CMOS process technology and some new CMOS circuit design technologies. The HM514256A offers Fast Page Mode as a high speed access mode.

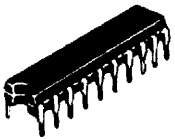
Multiplexed address input permits HM514256A to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

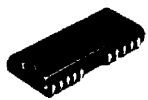
- Single 5V (± 10%)
- High Speed
  - Access Time . . . . . 60/70/80/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . 495/440/363/303/259mW (max.)
  - Standby Mode . . . . . 11mW (max.)
- Fast Page Mode Capability
- 512 Refresh Cycles . . . . . (8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$-Only Refresh
  - $\overline{CAS}$-Before-$\overline{RAS}$ Refresh

■ ORDERING INFORMATION

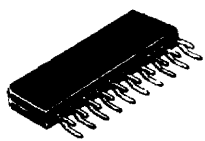
Part No.	Access	Package
HM514256API-6	60ns	300 mil 20 pin Plastic DIP (DP-20NA)
HM514256API-7	70ns	
HM514256API-8	80ns	
HM514256API-10	100ns	
HM514256API-12	120ns	
HM514256AJPI-6	60ns	300 mil 20 pin Plastic SOJ (CP-20D)
HM514256AJPI-7	70ns	
HM514256AJPI-8	80ns	
HM514256AJPI-10	100ns	
HM514256AJPI-12	120ns	
HM514256AZPI-6	60ns	400 mil 20 pin Plastic ZIP (ZP-20)
HM514256AZPI-7	70ns	
HM514256AZPI-8	80ns	
HM514256AZPI-10	100ns	
HM514256AZPI-12	120ns	



(DP-20NA)



(CP-20D)



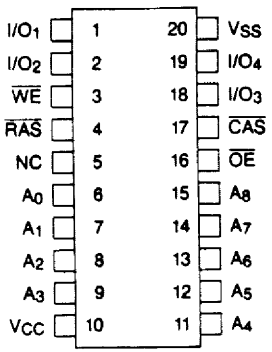
(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0-A_8	Address Input
A_0-A_8	Refresh Address Input
I/O_1-I/O_4	Data-In/Data-Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+5.0V)
V_{SS}	Ground

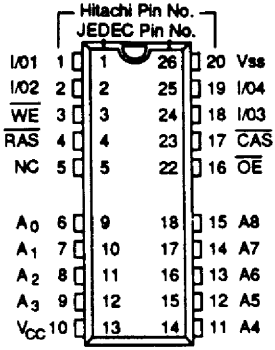
■ PIN ARRANGEMENT

• HM514256AP Series



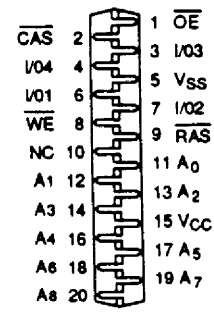
(Top View)

• HM514256AJP Series



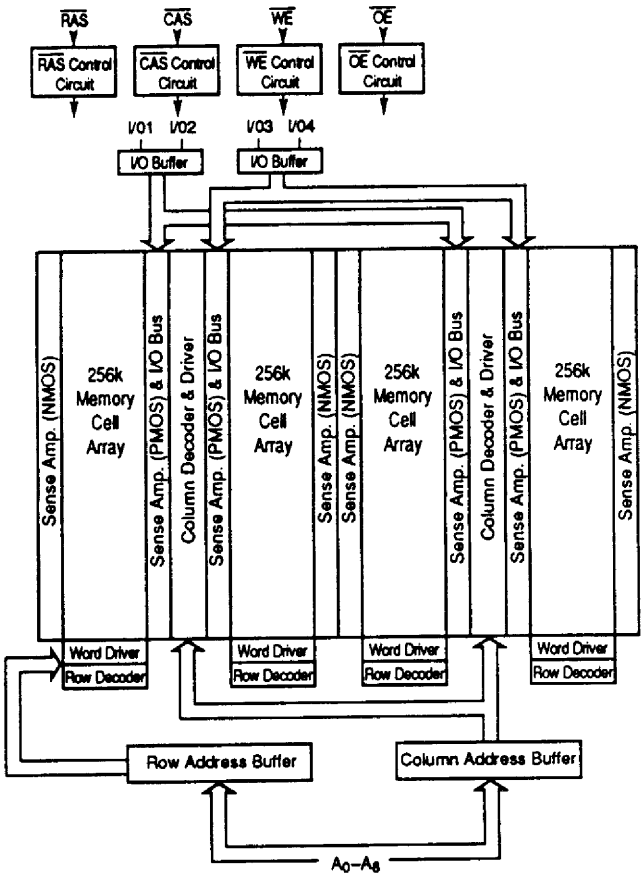
(Top View)

• HM514256AZP Series



(Bottom View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	-40 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = -40 to +85°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	-1.0	—	0.8	V	1
	(Others)	V_{IL}	-2.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC CHARACTERISTICS (T_a = -40 to +85°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = min.	—	90	—	80	—	66	—	55	—	47	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{OUT} = High-Z	—	2	—	2	—	2	—	2	—	2	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} -0.2V D_{OUT} = High-Z	—	1	—	1	—	1	—	1	—	1	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = min.	—	90	—	80	—	66	—	55	—	47	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} D_{OUT} = Enable	—	5	—	5	—	5	—	5	—	5	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = min.	—	80	—	70	—	66	—	55	—	47	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = min.	—	80	—	70	—	55	—	55	—	47	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	-10	10	-10	10	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V D_{OUT} = Disable	-10	10	-10	10	-10	10	-10	10	-10	10	μA	
Output High Voltage	V_{OH}	High I_{OUT} = -5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	Low I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-In, Data-Out)	$C_{I/O}$	—	10	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = -40°C to 85°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1], [14]

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Set-Up Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Set-Up Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{OE}$ to D_{IN} Delay Time	t_{ODD}	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time From D_{IN}	t_{DZO}	0	—	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ Delay Time From D_{IN}	t_{DZC}	0	—	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

• Read Cycle

Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Access Time From $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time From Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Access Time From $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	—	25	—	30	ns	
Read Command Set-Up Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	10	—	10	—	10	—	10	—	10	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	—	30	—	35	—	40	—	45	—	55	ns	
Output Buffer Turn-Off Time	t_{OFF1}	—	20	—	20	—	20	—	25	—	30	ns	6
Output Buffer Turn-Off to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	25	—	30	ns	6
$\overline{CAS}$ to D_{IN} Delay Time	t_{CDD}	20	—	20	—	20	—	25	—	30	—	ns	

• Write Cycle

Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-Up Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-In Set-Up Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-In Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

• Read-Modify-Write Cycle

Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read-Write Cycle Time	t_{RWC}	170	—	180	—	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	—	95	—	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	55	—	60	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55	—	60	—	70	—	80	—	95	—	ns	10
$\overline{OE}$ Hold Time From $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	25	—	30	—	ns	

• Refresh Cycle

Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Set-Up Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

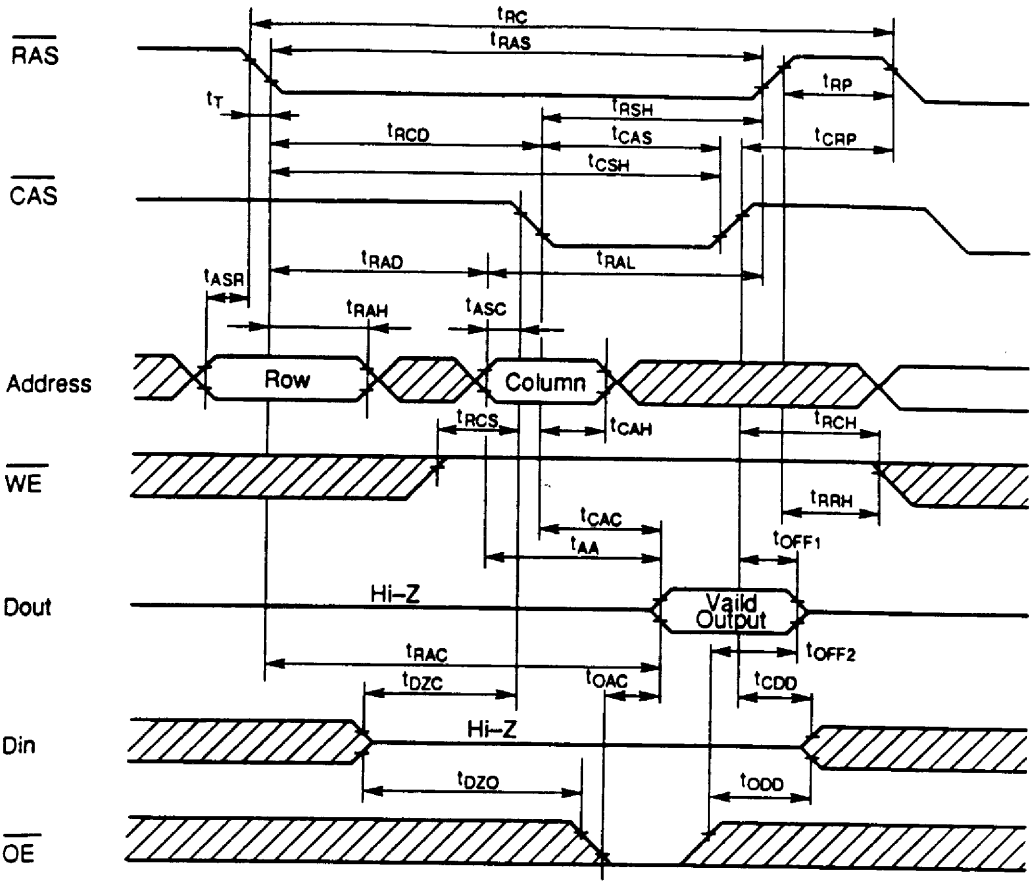
Parameter	Symbol	514256A-6		514256A-7		514256A-8		514256A-10		514256A-12		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Prechart Time	t_{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time From $\overline{CAS}$ Precharge	t_{ACP}	40	—	45	—	50	—	50	—	60	—	ns	
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	115	—	135	—	ns	

NOTES:

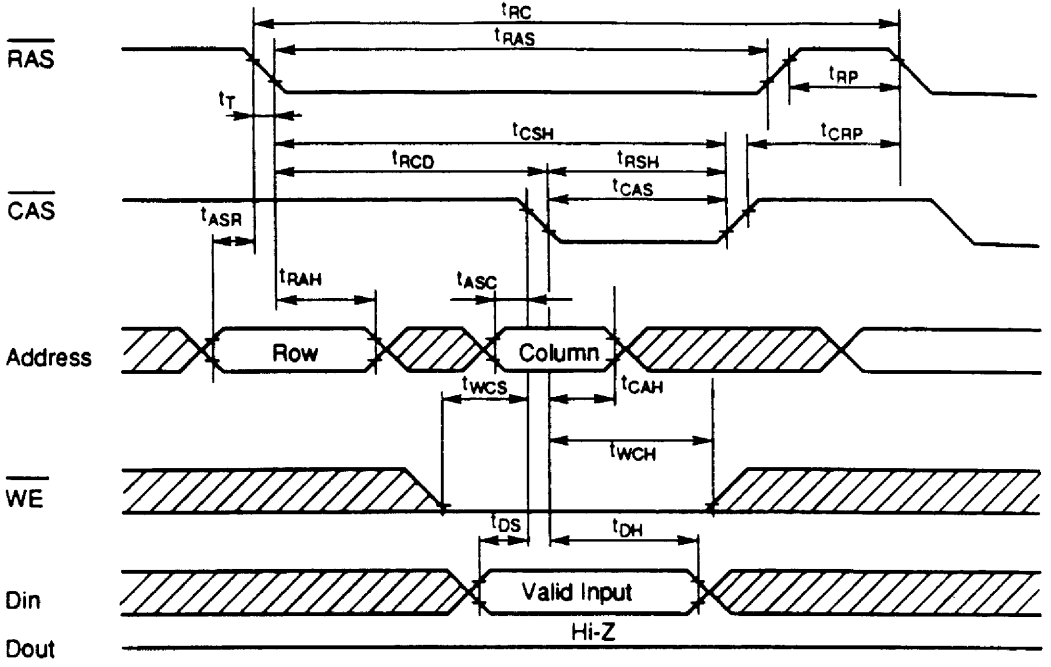
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

■ TIMING WAVEFORMS

• **Read Cycle**



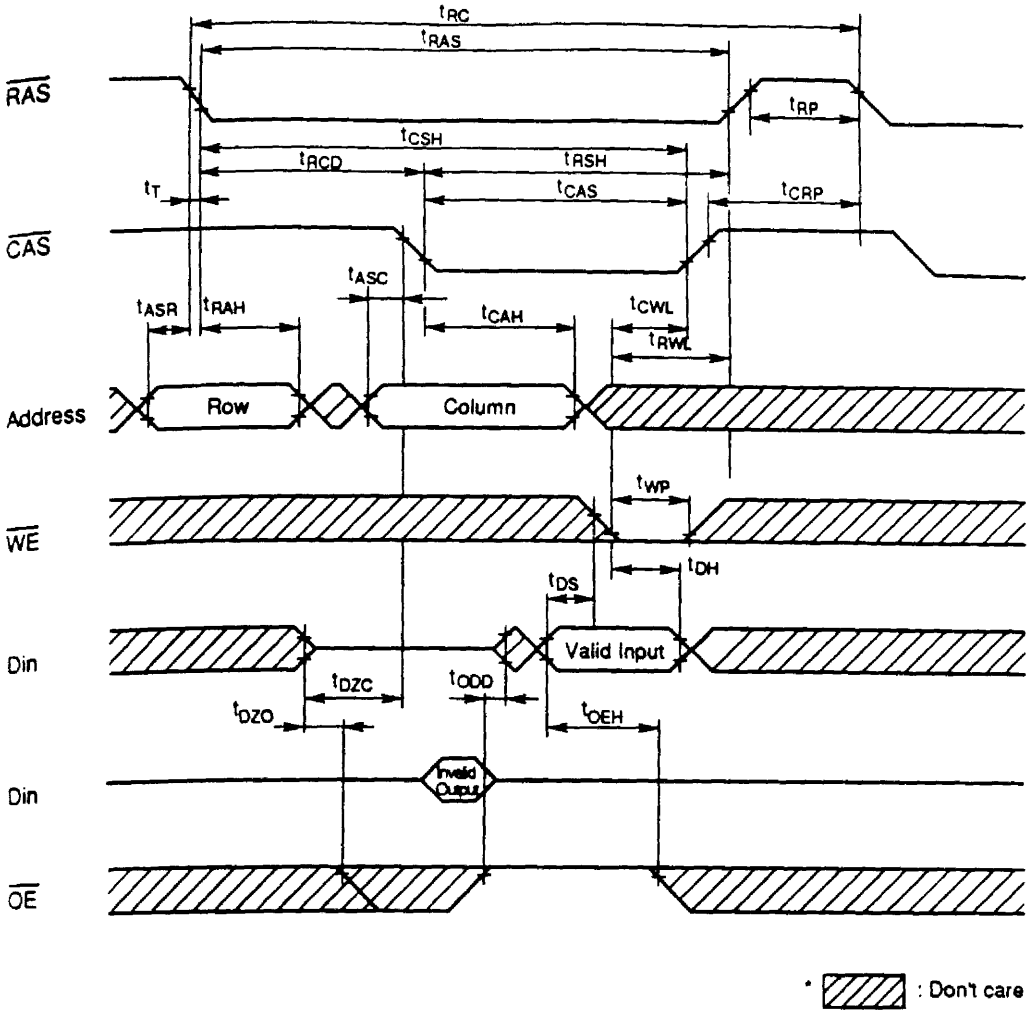
• **Early Write Cycle**



• $\overline{OE}$: Don't care

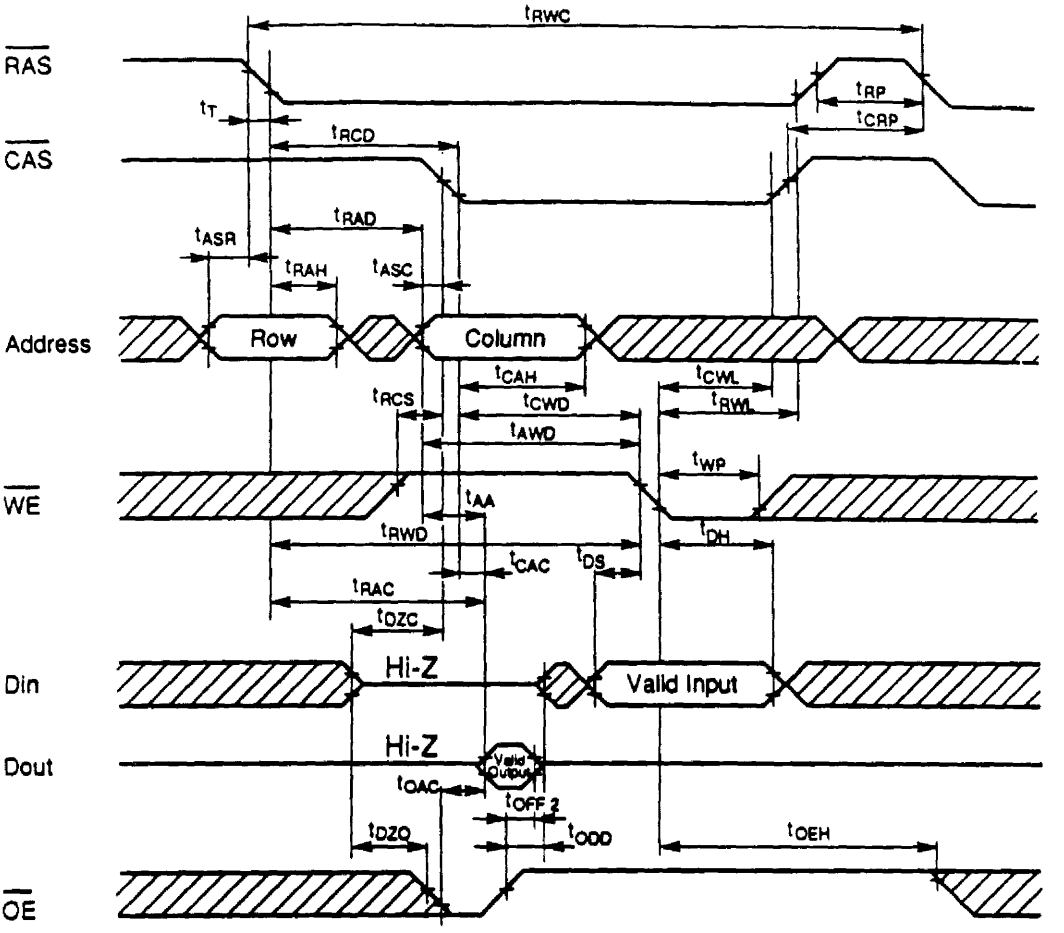
• ▨ : Don't care

• **Delayed Write Cycle**

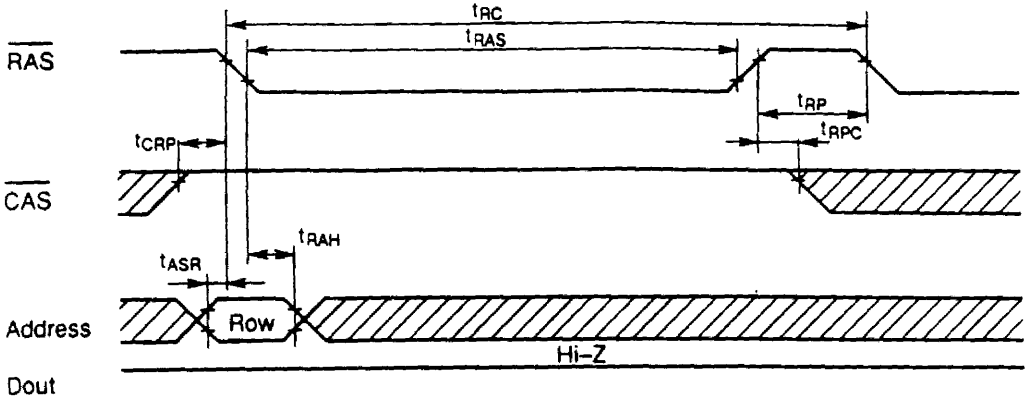


* ▨ : Don't care

• **Read-Modify-Write Cycle**



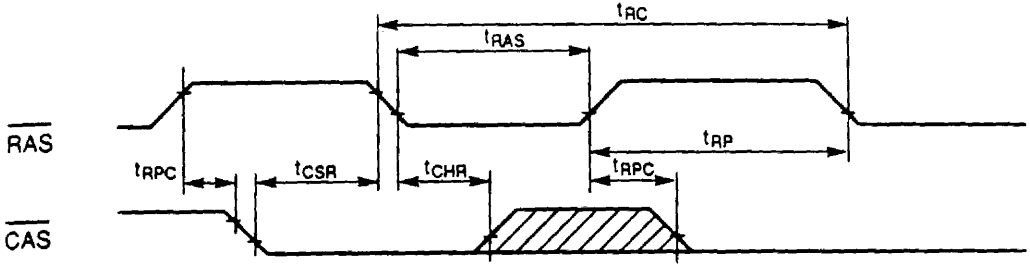
• **$\overline{RAS}$-Only Refresh Cycle**



1 $\overline{OE}$, $\overline{WE}$: Don't care

2 : Don't care

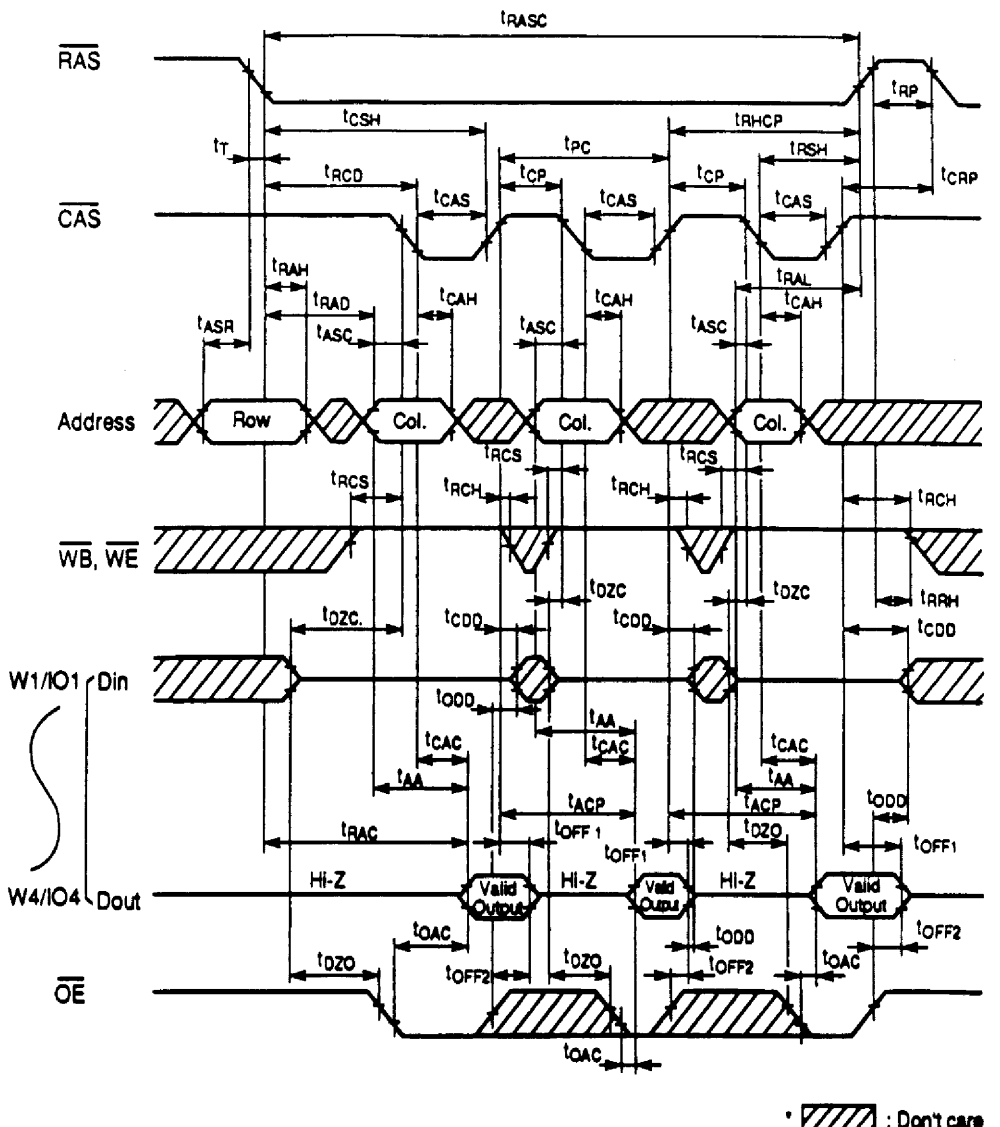
• **$\overline{CAS}$-Before $\overline{RAS}$ Refresh Cycle**



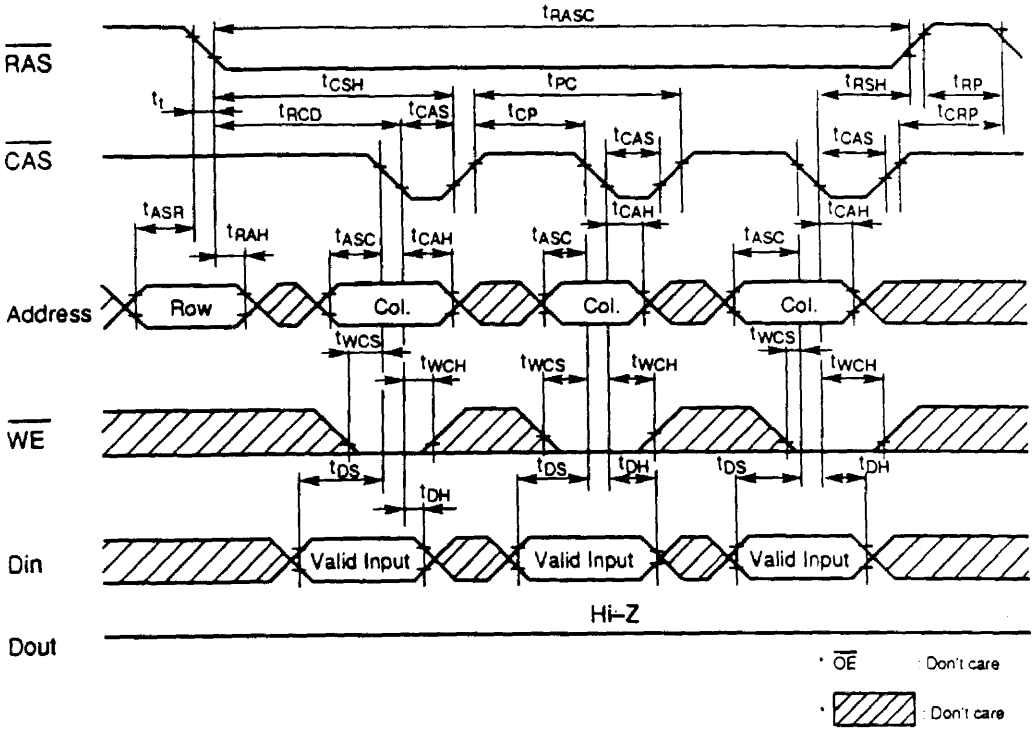
Address, Din, $\overline{WE}$: Don't care

Dout: High-Z

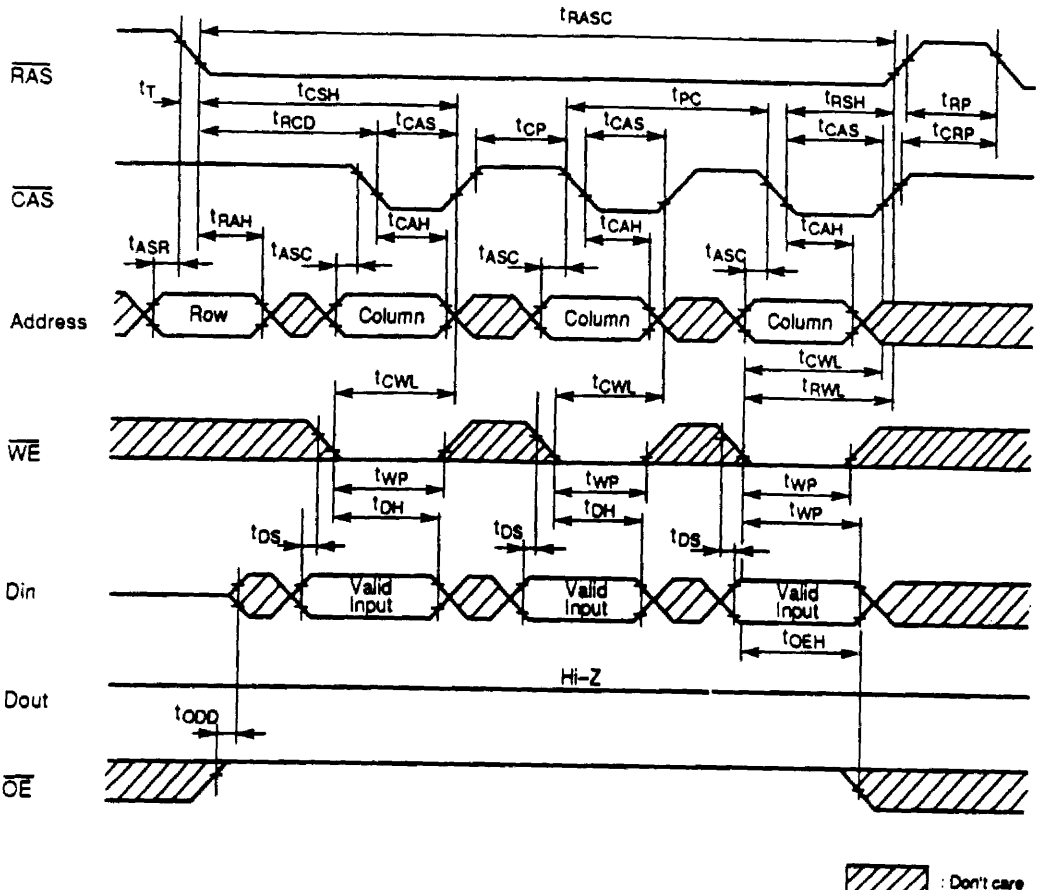
• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



• **Fast Page Delayed Write Cycle**



• **Fast Page Mode Read-Modify-Write Cycle**